EE / CPRE / SE 491 - sdmay20-38 iFPGA - Intermittent Intelligent FPGA Platform Week7 Report

11/4/19 - 11/8/19 Client: Henry Duwe

Faculty Advisor: Henry Duwe

Team Members:

Jake Tener - Team member, SW focus Jake Meiss - Team member, HW focus Andrew Vogler - Team member Zixuan Guo - Team member Justin Sung - Team member

Weekly Summary

The goal of this week was to determine if the only available microprocessor was feasible (8051), measure the in-rush power, and further refine the HW diagrams. Formulate a testing plan to guarantee verification and intended behavior when actually constructing the final prototype.

Past Week Accomplishments

- HW Justin Sung, Andrew Vogler, Zixuan Guo
 - Synthesized the microprocessor 8051 on the nano, realized that it takes up 87% of the PL space, and is thus unfeasible.
 - Slight changes to the HW flow since some of the IP cores had illogical connections to each other.

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- Power analysis Jake Meiss
 - Came up with methodology in order to get current measurements on an oscilloscope and not a multimeter
 - Researched possible solutions to problems with measuring extremely small drops in voltage with an oscilloscope
 - Make minor adjustments to power flow diagram to match new understandings of the system
- SW Jake Tener
 - Converted the SW ino Tensorflow Lite, stripped-down version that is feasible on the HW platform.

Pending Issues

No issues

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Jake Tener	SW	8	87
Jake Meiss	Platform/Harvester power analysis	8	87
Andrew Vogler	HW	8	87
Zixuan Guo	HW	8	87
Justin Sung	HW	8	87

Plans for Coming Week

- Research into the logistics of linking a TI MSP430 with the Microsemi IGLOO nano.
 - Data sharing protocol
 - o I2C or SPI
- Continue debugging the SW to successfully run in Tensorflow Lite.
- Obtain measurements for voltage drops and output currents of the FPGA running a flashing LED program during normal modes as well as boot up times and power consumption